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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,738	11/24/2003	Akio Sugi	FUJI:280	2747

7590 11/16/2004

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,738	SUGI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/26/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from Japanese Patent Application Nos. 2002-340186 filed on November 22, 2002 and 2003-176327 filed on June 20, 2003 which papers have been placed of record in the file.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-22 are, drawn to a semiconductor device, classified in class 257, subclass510 +.

II. Claim 23 is, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 221+

Inventions Group I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

In the instant case the product as claimed can be made by another and materially different process namely without the recited process step of filling the first and second trenches.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Marc A. Rossi (31,923) on November 10, 2004 a provisional election was made without traverse to prosecute the invention of Group I , claims 1-22.

Affirmation of this election must be made by applicant in replying to this Office action.

Claim 23 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

The drawings were received on May 26, 2004. These drawings are accepted by the draftsperson.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filed .11/ 24/ 2003

The references on PTO 1499 submitted on 11/24/2003 are acknowledged. All the cited references have been considered.

However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishima et al. (U.S. Patent No. 5,701,026, herein after Fujishima) in view of Saitoh et al. (U.S. Patent No. 6,693,338 herein after Saitoh).

With respect to claim 1 Fujishima describes a semiconductor device comprising: a semiconductor substrate, (Fujishima Fig. 1 # 101, col. 8 line 7) a trench formed in the substrate; (Fujishima fig. 1 # 102 , col. 8 line 6) at least one non-trench region surrounded by the trench; (Fujishima fig. 1 # 116, col. 9 line 26-27) an active region formed on the substrate over the trench for driving current as a semiconductor element, (Fujishima figure 1 # 107, col. 9 line 7) a first diffusion region formed at a bottom of the trench in the active region; (Fujishima figure 1 # 103, col.8 lines 7-8) and a second

diffusion region formed in the non-trench region,(Fujishima figure 1 # 101) wherein current is flow able between the first diffusion region and the second diffusion region, wherein the trench comprises a first trench section formed in the active region.

The limitation wherein current is flow able between first diffusion region and the second diffusion region is taken to be inherent function of the device and it is well settled law that " that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art , does not cause a claim drawn to it to distinguish over the prior art. In re Swinehart, 169 USPQ 226 (CCPA 1971) and In re Fuller 1929, C>D> 172, 388 O.G. 279.

Fujishima does not specifically describe a second trench section intersecting the first trench section to form a mesh pattern surrounding the non-trench region,

However Saitoh , a patent from the same filed of invention describes in figures 19 A to 31 and col. 29 lines 18 to 35 teaches a second trench section intersecting the first trench section to form a mesh pattern surrounding the non-trench region, wherein the first diffusion region is formed at the bottom of the first and second trench sections to balance the tradeoff relationship between the break down voltage and ON resistance i.e. simultaneously improve break down voltage and reduce ON resistance and also ease of manufacturing plurality of Reduced Surface field layer of the same depth to ensure same break down voltage.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Saitoh's teaching of a second trench section intersecting the first trench section to form a mesh pattern surrounding the non-trench region, wherein

the first diffusion region is formed at the bottom of the first and second trench sections in Fujishima's device . The motivation to undertake the above combination is to balance the tradeoff relationship between the break down voltage and ON resistance i.e. simultaneously improve break down voltage and reduce ON resistance and also ease of manufacturing plurality of Reduced Surface field layer of the same depth to ensure same break down voltage. (Saitoh, col.1 lines 30-35 and col. 3 lines 4-6).

With respect to claim 2 Fujishima describes the semiconductor device as claimed in claim 1, wherein the trench further includes at least one third trench section connected to the first and second trench sections forming the mesh pattern to divide the non-trench region into a plurality of smaller regions. (Saitoh fig. 24 F, col. 25 lines 25 to 44).

With respect to claim 3 Fujishima describes the semiconductor device as claimed in claim 2, further including: an electrode electrically connected to the second diffusion region, (Saitoh , figure 24 F # 17, col. 7 lines 49-50) and a contact section electrically connected to the second diffusion region and the electrode, wherein the contact section is disposed over and contacting all of the smaller regions in the non-trench region. (Saitoh figure 27 B 17 contacting 12 and 13 portions outside trench).

With respect to claim 4 Fujishima describes the semiconductor device as claimed in claim 2, wherein the third trench section extends parallel to the first trench section. (Saitoh fig. 24 f 13 is parallel to 18).

With respect to claim 5, Fujishima describes the semiconductor device as claimed in claim 2, wherein the third trench section extends parallel to the second trench section. (Saitoh fig. 24 F 12 parallel to 18) .

With respect to claim 6, Fujishima describes the semiconductor device as claimed in claim 2, wherein the third trench section extends diagonally to both the first and second trench sections. (Saitoh fig. 24 F 13 also extends diagonal to 18 and 12 in mesh embodiment , col. 29 line 30) .

With respect to claim 7, Fujishima describes the semiconductor device as claimed in claim 2, wherein the third trench section comprises a combination of two or three subsections, each of which extends parallel to the first trench section, parallel to the second trench, or diagonally to both the first and second trench sections. (Saitoh figure 24 F # 13 at least two sub-sections and rest rejected for reasons set out under claims 4-6 above).

With respect to claim 8 Fujishima describes the semiconductor device as claimed in claim 2, wherein the semiconductor device is a trench lateral transistor composed of at least the semiconductor substrate, the first and second diffusion regions, the first diffusion region driving current as a transistor, a gate insulator film formed inside the trench, a first conductor formed inside the gate insulator film, a second conductor formed inside the first conductor in the active region with an interlayer insulator film interposed there between and electrically connected to the first diffusion region, a first electrode penetrating through the interlayer insulator film electrically connected to the second diffusion region, and a second electrode entering through the interlayer

insulator film to electrically connect to the second conductor. (Saitoh figure 24 F # 13 at least two sub-sections and rest rejected for reasons set out under claims 1-6 above).

With respect to claim 9 Fujishima describes the semiconductor device as claimed in claim 8, wherein the third trench section extends parallel to the first trench section. (rejected for reasons stated under claim 4 above)..

With respect to claim 10 Fujishima describes the semiconductor device as claimed in claim 8. wherein the third trench section extends parallel to the second trench section. (rejected for reasons Stated under claims 5 and 6 above).

With respect to claim 11 Fujishima describes The semiconductor device as claimed in claim 8, wherein the third trench section extends diagonally to both the first and second trench sections. (rejected for reasons stated under claim 5 above).

With respect to claim 12 Fujishima describes the semiconductor device as claimed in claim 8, wherein the third trench section comprises a combination of two or three subsections, each of which extends parallel to the first trench section, parallel to the second trench, or diagonally to both the first and second trench sections. (rejected for reasons et out under claim 7 above).

With respect to claims 13 and 14 Fujishima describe the semiconductor device as claimed in claim 8, wherein the second diffusion region is a drain region (Saitoh figs. # 16, col. 7 line 50) and the first diffusion region is a source region. (Saitoh figs. 13 , col. 7 line 45, nomenclature first and second interchangeably used).

With respect to claim 15 Fujishima describes the semiconductor device as claimed in claim 13, wherein the inside of the third trench section is filled with the first

conductor (Fujishima fig.1 # 103, col. 8 line 11) with the gate insulator film interposed there between, (Fujishima fig. 1 # 104col.8 line 12) and the first conductor in the third trench section from and the first electrode are insulated from each other by an interlayer insulator film. (Saitoh 24 F # 12/,13 and 17 insulated from each other by insulator 14).

With respect to claim 16 Fujishima describes the semiconductor device as claimed in claim 14, wherein the inside of the third trench section is filled with the first conductor with the gate insulator film interposed there between, and the first conductor in the third trench section and the first electrode are insulated from each other by an interlayer insulator film. (Saitoh figure 39 , col. 35 lines 34 to 50)

With respect to claim 17 Fujishima describes the semiconductor device as claimed in claim 8, wherein an interlayer insulator film thicker than the gate insulator film is provided along a part of a side section of the first trench section. (Saitoh fig. 39 50 is thicker than 14).

With respect to claim 18 Fujishima describes the semiconductor device as claimed in claim 1, wherein a width of the second trench section is narrower than a width of the first trench section.(Fujishima figure 1) .

With respect to claims 19 and 20 Fujishima describes the semiconductor device as claimed in claim 1, wherein the second diffusion region is a drain region and the first diffusion region is a source region, (region (Saitoh figs. # 16, col. 7 line 50) (Saitoh figs. 13 , col. 7 line 45, nomenclature first and second interchangeably used) and further including a first conductor formed on the inside of the first and second trench sections with an insulator film interposed there between (Saitoh figure 39 , col. 35 lines

34 to 50) and a second conductor electrically connected to the first diffusion region formed on the inside of the first conductor in the first trench section with an interlayer insulator film disposed there between. (Saitoh figs. 24 F 27 B , etc.)

With respect to claims 21 and 22 Fujishima describes the semiconductor device as claimed in claim 19, further including an interlayer insulator film thicker than the insulator film in each of the first trench section and the second trench section on each side section of the first trench section and on each side section or at a bottom of the second trench section. (Saitoh 30 th embodiment figure 41 B # 57 thicker than # 50 portion under # 17).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

November 12, 2004.